

Convolution Assisted Polar Encoder with Flexible Iterative Decoding for Forward Error Correction in Wireless Communication Incorporated in Fpga

T. Ranjitha Devi^{*1}, and Dr. C. Kamalnathan²

Abstract—The effectiveness of Forward Error Correction (FEC) approaches depends on the coding scheme and code length, which result in increasing processing latency and delay. Hence, a novel Convolution Assisted Polar Encoder with Flexible Iterative Decoding (CAPE-FID) is proposed to improve communication efficiency by reducing latency and retransmission. Existing approaches use longer block length codes for error correction and seamless communication, but it unnecessarily increases bits, affecting bandwidth and data rate. Hence, a novel Polarized Convolutional Encoder (PCE) is introduced, which uses Adaptive Frozen Polar Coding (AFPC) and Convolution coding to eliminate unnecessary high redundancy from the input data, improving both the useful data rate and the efficient use of available bandwidth. Existing CRC algorithms' lower-degree polynomials during divisional detection cause collisions, thus incorrectly identifying error-free data, causing overhead and affecting data transmission overall. Hence, a novel Flexible Turbo Decoder (FTD) is introduced, which uses Reed-Solomon Euclid (RSE) Code and Sequential Concatenated Turbo coding to reduce packet loss and improve data transmission quality and network congestion handling. Finally, the error-corrected data is decoded using Adaptive Polar Coding with reversed polarization transformation (APC-Rpt). The results show that the proposed method has improved efficiency and reduced retransmission rate, latency and error rates.

Index Terms—Forward Error Correction, Convolution codes, Polar Codes, Euclidean algorithm, Reed-Solomon code, Turbo coding

I. INTRODUCTION

Forward Error Correction (FEC) is a key technique in wireless communication that improves data accuracy and reliability by adding redundant bits at the transmitter. These bits enable the receiver to detect and correct errors caused by fading, noise, interference, and signal attenuation, without requiring retransmission. By encoding data with error-correcting codes and transmitting both the data and redundancy, FEC mitigates channel-induced errors and ensures more consistent performance [1-4].

FEC enhances wireless communication reliability by reducing bit error rate and mitigating channel defects, enabling data recovery even with weak or corrupted signals. This is vital for real-time applications or scenarios with power or latency constraints that preclude retransmission. Common FEC

techniques include polar, Reed-Solomon, Low-Density Parity-Check (LDPC), and convolutional codes, each offering different trade-offs between error correction, complexity, and efficiency. Widely used in digital broadcasting, Wi-Fi, cellular networks (3G, 4G, and 5G), satellite communication, and wireless sensor networks, FEC ensures stable and robust connections even in challenging wireless environments [5-8].

Retransmission addresses the challenges of defective wireless channels by recovering lost or corrupted packets, improving reliability, and ensuring correct data delivery. However, excessive retransmissions can increase delays and reduce throughput, making process optimization vital for balancing reliability and efficiency. Protocols like Automatic Repeat reQuest (ARQ) trigger retransmission when ACK or NAK responses are not received. Error correction systems must adapt to unstable channel conditions, adjusting decoding settings in real time, which is a challenge under channel variability. Multipath propagation and interference from neighboring signals can further reduce effectiveness, requiring advanced decoding to separate interference from the intended signal. Achieving a balance between error correction capabilities and processing efficiency is difficult, as stronger techniques often demand significant resources [9-12].

High-speed communication systems use FEC to maintain reliability at high data rates, but FPGA (Field Programmable Gate Array)-based implementations face challenges in managing clock domains, serialization/deserialization, and synchronization. Compared to ASICs (Application-Specific Integrated Circuit), FPGAs generally consume more power, requiring optimization techniques such as reducing unnecessary computations, using low-power resources, and implementing power-gating. Validating FEC accuracy and performance on FPGAs is also complex due to their concurrent nature, demanding extensive test benches, simulations, and fault scenario validation [13-15]. Despite ongoing research, many aspects of wireless communication still need improvement for effective data transfer without losses, highlighting the need for a novel FEC-based approach. The main contributions of this paper are:

- To reduce the unnecessary high redundancies added to the input data, a novel PCE is introduced, which improves the useful data rate and effective usage of available bandwidth.

- To avoid packet loss and to improve the overall data transmission quality, a novel FTD is introduced, which detects, locates and corrects the errors based on the sequential manner.

The proposed work is divided into five sections, the first is

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an introduction and the second is a review of the literature. Section 3 encapsulates the proposed method discussing sub modules. Performance and comparative analysis are covered in Section 4. Section 5 delves deeply into the work's conclusion.

II. LITERATURE SURVEY

Vinodhini et al. [16] suggested a Transient Error Correction (TEC) coding technique for a low-power data link layer in Network on Chip (NoC) for error correction capability with minimal hardware complexity. Validated through simulations and realistic traffic patterns, it achieved more reliable transmission at lower link swing voltages and reduced power consumption compared to the Hamming product code, albeit with a slight increase in codec delay and router latency. However, it did not fully balance error correction with bandwidth efficiency.

Syed Mohsin Abbas et al. [17] outlined the GRAND-MO algorithm's hardware architecture for decoding linear block codes in memory-based communication channels, which was enhanced for simplifying hardware implementation. The improved VLSI design achieved higher throughput and decoding gains compared to both the GRANDAB and BCH decoders, though it still requires adaptation to varying channel conditions for optimal error correction.

Konda Nandan Kumar et al. [18] proposed a Matrix-based error correction and parity-sharing approach for detecting and rectifying adjacent and certain multiple-bit faults. By computing specific bits using a DNA-shaped curve within the matrix, the approach reduced power, area, and latency, making it suitable for memory systems, though some residual errors remained uncorrected.

Qilin Zhang et al. [19] created a deep learning-based, SPA-based, data-driven method for decoding CRC codes that coupled internal trainable parameter optimization with learning. A loss function based on a weighted average of negentropy was employed for evaluating the Gaussianity and binary cross-entropy (BCE) of the decoder output. Though the proposed strategy with deep unfolding and negentropy-aware loss function enhanced the bit error rate, it failed to ensure interoperability between different systems.

Linfang Wang et al. [20] presented cyclic redundancy check (CRC) aided probabilistic amplitude shaping (PAS) on a trellis-coded modulation (TCM) to achieve the short-block length random coding union (RCU) condition. The transmitter's distribution matcher first encoded similar message bits to produce amplitude symbols with the necessary distribution, then encrypted using a CRC, and finally, encoded and modulated using Ungerboeck's TCM scheme. However, there was a trade-off between the level of redundancy and the achievable error correction capability.

Svitlana Matsenko et al. [21] evaluated indivisible codes for binary symmetric channels using the average probability method and implemented a fractal decoder in FPGA with multilayer PAM and grey code mapping for short-reach optical interconnects. While effective for end-to-end data management with uniform structure and high speed, the approach was inefficient in handling burst errors and required improved code mapping.

Bai et al. [22] suggested a brand-new photonic spectrum-spreading phase-coding-based joint radar and communication (JRC) system operating at millimeter waves. The convergence of spectrum-spreading multiplexing and photonic microwave phase-coding techniques was the key to the system. By orthogonalizing the transmission data and the radar signal, spectrum-spreading multiplexing significantly reduces mutual interference. Furthermore, spectrum-spreading multiplexing enhance communication's anti-jamming, anti-noise performance as well as radar's peak sidelobe ratio. However, nonlinear distortions were produced by the radar's power amplifier (PA).

Bhargavi et al. [23] provided a technique for utilizing the H-Matrix as a detection and repair mechanism for several instances of double adjacent faults. Three distinct H-Matrix based codes with varying quantities of parity bits were presented and compared for various parameters using three different parity check matrices. To minimize the complexity of encoder and decoder circuits, the H-Matrix was built with fewer ones and less redundancies. However, it only focuses on correcting errors of up to 8 bits caused by double adjacent errors.

Prathyusha et al. [24] introduced a Matrix based technique for error detection and correction for memories, using power and stoppage to concentrate on the equality bits. The approach was effective in scenarios with limited speed and parity bits, employing both row and column decoders for address control during read and write operations. However, the system's complexity resulted in higher power consumption and longer processing delays.

Wang et al. [25] proposed deep error-correcting output codes, integrating deep, online, and ensemble learning. Incremental SVMs acted as weighted links between successive layers, with each ECOC module representing a layer pair. Class labels were used in pre-training to initialize the network, enabling effective performance, particularly for large-scale tasks. However, the method does not fully address scalability or computational efficiency for more complex datasets.

The literature review shows that prior works faced various limitations: [16] struggled to balance error correction and bandwidth efficiency; [17] underperformed across channel conditions; [18] failed to reduce residual errors; [19] lacked interoperability; [20] faced a redundancy-error correction trade-off; [21] inadequately handled burst errors and required better code mapping; [22] suffered from radar's power amplifier induced nonlinear distortions; [23] was limited to correcting small double-adjacent errors; [24] had high power use and delays due to complexity; and [25] lacked scalability and computational efficiency for large datasets. These gaps highlight the need for a novel approach to improve wireless communication effectiveness.

III. CAPE-FID

The amount of redundant bits added by the chosen coding scheme and the code length determine how well FEC approaches repair errors. The current FEC methods increase processing latency and delay by requiring more computational resources and a lower usable data rate. Hence, a novel

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Convolution Assisted Polar Encoder with Flexible Iterative Decoding is developed to solve the drawbacks of the current FEC approaches used in wireless communication and enhance its communication efficiency by lowering latency and retransmission. The current methods employ longer block length codes in an attempt to increase error correction capacity and facilitate smooth system-to-system communication, but doing so unnecessarily takes up more bits overall, which ultimately reduces available bandwidth and the required useful data rate. Hence, a novel Polarized Convolutional Encoder is presented, in which the original data is first encoded using Adaptive Frozen Polar Coding in which the polarization transformation approach encodes the original input bits along with some added frozen bits only based on the length of the original data thereby avoiding unnecessary block lengths. After this, the transformed bits from the polar code undergo additional encoding using convolution codes that employ generator polynomials to control the output bit length and provide redundancy to the data stream, which facilitates error identification and correction at the receiver end. With this PCE, the unnecessary high redundancies added to the input data are reduced thus the useful data rate and effective usage of available bandwidth are improved.

Moreover, in congested network conditions, retransmission occurs due to packet loss, causing data loss at the receiver end. Existing error approaches, like CRC algorithm, which struggles to handle congestion, resulting in packet drop and lost data. Since different data sequences can produce the same CRC value in the existing CRC algorithms, the lower-degree polynomials used during divisional detection at the receiver end are more likely to collide. As a result, they mistakenly identify error-free data as erroneous, adding overhead to the error correction technique in the next step and affects the data transmission overall. Hence, a novel Flexible Turbo Decoder is presented at the receiver end, whereby Turbo coding schemes and modified Reed-Solomon (RS) code are used for error detection and correction. Once the data is received at the receiver end, the Reed-Solomon Euclid (RSE) Code is used to identify errors. This reduces the incorrect identification of error-free data and eliminates the need for error correction overhead by calculating syndromes based on the received codeword using the generator polynomial of the RS code and locating the error using the Euclidean algorithm. Following error detection, the error correction process uses Sequential Concatenated Turbo coding, which uses an iterative error correction approach in interaction with the error detection technique (RSE) in the previous stage and corrects the erroneous bits in the incoming bits in a sequential manner. This prevents packet loss and enhances the overall data transmission quality with improved network congestion handling. Finally, the error-corrected data is decoded using APC-Rpt.

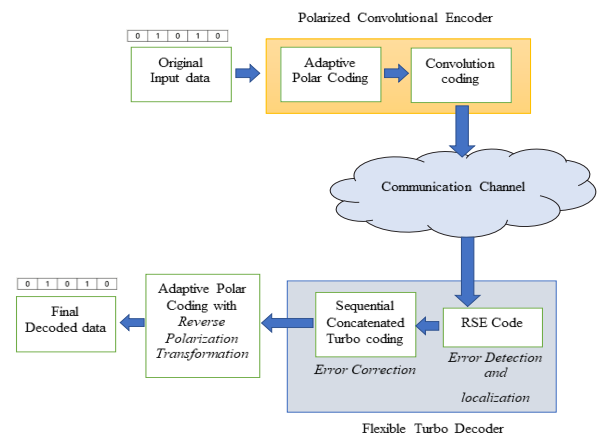


Fig. 1. Block Diagram of the proposed system

Fig. 1. displays the block diagram of the proposed model, which includes the sender side, the communication channel, and the receiver end. Initially, the original input data is sent to the PCE, which includes Adaptive polar coding and convolution coding for encoding the original data by this the unnecessary high redundancies added to the input data are reduced. Then, the encoded data are sent to the FTD placed at the receiver end through the communication channel for error detection and correction. First, the RSE Code is employed to detect errors followed by Sequential Concatenated Turbo coding for error correction. Finally, the error-corrected data is decoded using APC-Rpt.

A. Polarized Convolutional Encoder

In wireless communication, FEC is a technique that increases dependability by adding redundant information to the sent data. This way, faults can be corrected by receivers without requiring retransmission. This aids in the fight against problems like interference and noise in wireless channels. Initially, the original input data is sent to the PCE, which consists of AFPCand convolution codes, is used to reduce the unnecessary high redundancies added to the input data thus the useful data rate and effective usage of available bandwidth are improved.

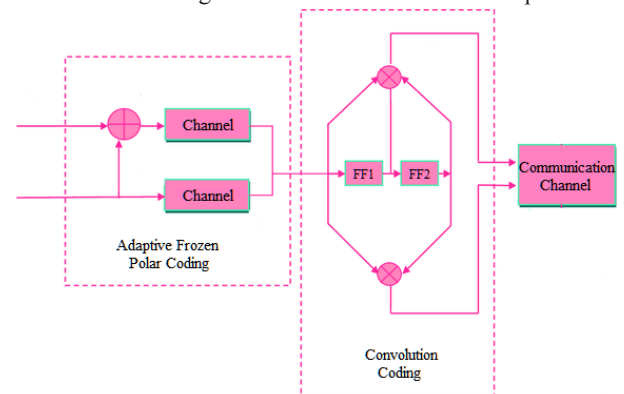


Fig. 2. Polarized Convolutional Encoder

Fig. 2. displays the PCE of the proposed system. The output from the polar encoder is applied to the convolutional encoder during data transmission to create an output at the transmitter

side. Additionally, the convolutional encoder's output is sent over a communication channel, and the recipient side decodes the data to obtain it.

First, the AFPC is used to encode the initial input data. Using a process called polar coding, information is converted into polarized bits, some of which are labelled as "frozen" and some as "information". By selectively activating or deactivating specific bits in the original data sequence, the polarization transformation essentially produces a polarized version of the data. The adaptive feature of frozen bit insertion is the main novelty in this case. The encoder dynamically decides the number of frozen bits based on the length of the original data, as opposed to employing a fixed set of frozen bits for all data lengths. The encoding process is represented by the equation (1).

$$x = u \times F + f \quad (1)$$

where, u is the original input data bits, x is the encoded polarized bits, f is the frozen bits, and F is the transformation matrix that polarizes the original data. This adaptive approach helps avoid unnecessary block lengths, optimizing the encoding process for each specific data sequence.

Following the polarization transformation, convolutional codes are used to further encode the polar code's transformed bits. Generator polynomials are used by convolutional codes to produce redundant bits and control the output bit stream's length. The encoder controls the amount of redundancy introduced to the data stream by varying the generating polynomials. The convolutional encoding process is represented as in equation (2).

$$c = x' \times G \quad (2)$$

where, x' is the encoded polarized bits after polar coding, c is the convolutional encoded bits, and G is the generator polynomial matrix. Convolutional coding adds redundancy, which facilitates error detection and correction at the receiver end. Convolutional codes are appropriate for wireless communication systems because of their well-known capacity to identify and correct errors in noisy communication channels. The overall encoding process involves both polar coding and convolutional coding is given in equation (3).

$$c = (u \times F + f) \times G \quad (3)$$

Thus, the PCE reduces excessive redundancy that are introduced to the input data that aren't necessary. This reduction in redundancies translates to improved useful data rate and more effective use of available bandwidth. By adding only necessary redundancy to the data stream, the communication system's overall efficiency is improved. Next, the encoded data is sent to the FTD at the receiver end through the communication channel for error detection and correction, as explained in section 3.2.

B. Flexible Turbo Decoder (FTD)

A FTD is a type of decoder designed to handle FEC in wireless communication systems, in which the error detection and correction are done with modified Reed-Solomon (RS) code and Turbo coding schemes. By employing a unified design, it is able to decode a variety of FEC codes, such as Turbo, Low-Density Parity-Check (LDPC), and Polar codes. In

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various communication circumstances, this adaptability enables dependable and efficient data delivery.

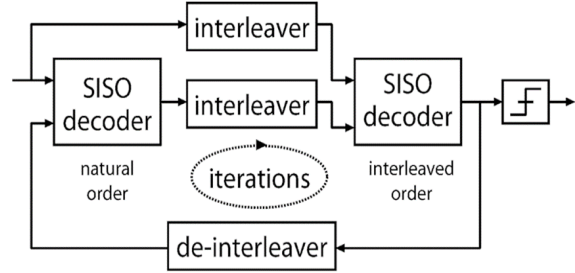


Fig. 3. Turbo Decoder

Fig. 3. displays the Turbo Decoder of the proposed system. The iterative decoding process is the essential component of a Turbo Decoder. This involves two iteratively exchanging Soft-Input Soft-Output (SISO) component decoders. Based on the output of the previous decoder and the received signal, each decoder improves its estimation of the transmitted data. With each iteration, this back-and-forth procedure improves the precision of the decoding.

When the transmitted data is received at the receiver end, it undergoes error detection using the RSE Code. The generating polynomial of the RS code is used by the RSE code to compute syndromes based on the received codeword. These syndromes basically serve as error detectors, indicating whether errors are present in the received data. The codeword $c(x)$ of RS code can be expressed mathematically as in equation (4).

$$c(x) = g(x) \times m(x) + e(x) \quad (4)$$

where, $g(x)$ is the generator polynomial of an RS code, $m(x)$ is the message polynomial, and $e(x)$ is the error polynomial. Based on the determined syndromes, the Euclidean method is then applied to detect and identify errors in the received data. The steps of the Euclidean algorithm involve repeated division with remainder until the remainder becomes zero. The receiver distinguish between data that has to be corrected and data that is error-free by successfully detecting errors at this stage. Mathematically, the algorithm is expressed as in equation (5).

$$gcd(a, b) = gcd(b, a \bmod b) \quad (5)$$

This lowers the possibility that error-free data will be mistakenly identified and also saves needless overhead in the subsequent error correction process.

After error detection using the RSE code, the next step is error correction using Sequential Concatenated Turbo Coding, an iterative error correction scheme that works in conjunction with the error detection method used in the previous stage (RSE). Using a step-by-step methodology, it corrects the erroneous bits in the incoming data stream, continuously improving the error correction procedure. Sequential Concatenated Turbo Coding can efficiently handle packet loss and enhance overall data transmission quality by iteratively refining error correction based on prior detections, especially in situations with network congestion or other unfavourable conditions.

After error correction is finished, APC-Rpt is used for the final decoding of the error-corrected data. The error-corrected

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data is decoded using Adaptive Polar Coding, which modifies the decoding procedure according to the incoming signal's properties. In order to guarantee a correct reconstruction of the original data, reversed polarization transformation is used to reverse the polarization transformation that was applied during the encoding stage. This is expressed in equation (6).

$$u' = x' \times F' \quad (6)$$

The accurate decoding of the error-corrected data is ensured by this last decoding step, making it suitable for transmission or additional processing.

Thus, the Flexible Turbo Decoder scheme combines error detection with RSE Code, iterative error correction with Sequential Concatenated Turbo Coding, and final decoding with Adaptive Polar Coding to effectively handle errors and improve data transmission quality in wireless communication systems. Each step contributes to reducing latency, avoiding packet loss, and enhancing the overall efficiency of the communication system.



Fig. 4. Overall Architecture of the proposed model

Fig. 4. illustrates the overall architecture of the proposed model. The original data is first delivered to the PCE, which uses convolution coding and adaptive polar coding to encode the original data. The encoded data are then transmitted via the communication channel (Noisy channel) to the FTD, which is positioned at the receiver end, where RSE Code is used for error detection and Sequential Concatenated Turbo coding is used for error correction. Overall, the proposed error correction approach enhanced the useful data rate with available bandwidth, and data transmission efficiency, and also reduced retransmission.

IV. RESULT AND DISCUSSION

This section includes a thorough discussion of the implementation results, as well as the performance of the proposed CAPE-FID method, and a comparison to ensure that the proposed system successfully performed FEC in wireless communication incorporated in FPGA.

A. System configuration

The proposed system is simulated in MATLAB R2023a with the HDL Coder extension for FPGA implementation on a Xilinx Zynq-7000 series platform [30], with Windows 10 (64-bit) OS, Intel(R) Core (TM) i3-4130 CPU @ 3.40GHz processor, and 8GB RAM.

B. Performance metrics of the proposed system

In this section, a detailed explanation of the effectiveness of the suggested technique and the achieved outcome were

explained. Implementation results are analyzed in terms of throughput and latency, optimized for the target device's parallel processing and efficient logic resources.

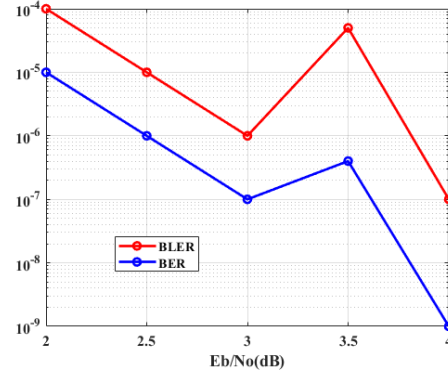


Fig. 5. BER, and BLER of the proposed system

The Bit Error Rate (BER) and Block Error Rate (BLER) performance of the proposed system, shown in Fig. 5. is evaluated across various SNR per bit (E_b/N_0) values. The BER achieves a maximum value of 10^{-5} at 2 dB and reaches a minimum of 10^{-9} at 4 dB, as the APC-Rpt enhances decoding efficiency, maximizing the likelihood of accurately recovering transmitted information and contributing to a lower BER. Meanwhile, the BLER reaches a maximum of 10^{-4} at 2 dB and decreases to a minimum of 10^{-7} at an SNR of 4 dB. This reduction in BLER at higher SNR values is largely due to the effectiveness of the RSE Code for error detection, which minimizes false positives by accurately identifying errors and reducing the likelihood of mistakenly flagging error-free blocks as erroneous.

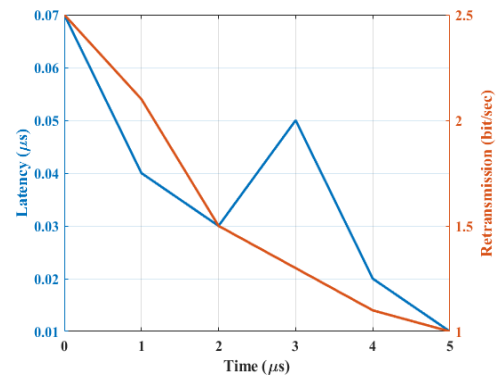


Fig. 6. Latency and retransmission of the proposed system

Fig. 6 illustrates the latency and retransmission performance of the proposed system across varying time periods. At a time interval of 5 μs , the latency reaches a minimum of 0.01 μs , while a maximum latency of 0.04 μs is observed at a time interval of 2 μs . This latency behavior of alternation between 2 to 4 μs is due to the system's CAPE-FID which optimizes both encoding and decoding processes, thereby reducing overall processing time, minimizing latency. Meanwhile, the retransmission rate peaks at 2.1 bits/sec at 1 μs , and decreases

to 1 bit/sec at $5 \mu\text{s}$. Sequential Concatenated Turbo Coding, employed for iterative error correction, allows the decoder to refine its estimation of the transmitted data progressively over multiple iterations. The reduction in retransmissions enhance the reliability of the received data and lead to more efficient use of the communication channel.

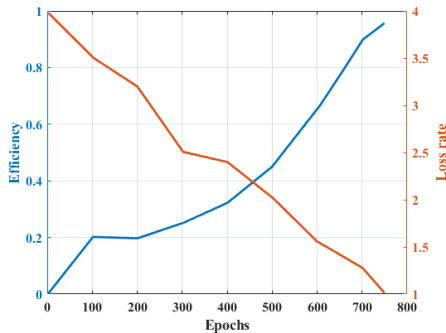


Fig. 7. Efficiency and loss rate of the proposed system

Fig. 7 presents the efficiency and loss of the proposed method across varying numbers of epochs ranging from 0 to 700. The system achieves a maximum efficiency of 0.94% at 700 epochs and a minimum efficiency of 0.45% at 500 epochs. This trend is attributed to CAPE-FID, which optimizes bandwidth utilization and by fine-tuning the encoding and decoding, it minimizes redundancy and increases efficiency. Meanwhile, on epoch 500, the system experiences a maximum loss rate of 2%, and a minimum of 1% at epoch 700. The loss reduction is primarily attributed to the PCE which enhance the error correction capabilities of the encoding process. Thus with increasing epochs, performance is increased with high efficiency and reduced loss rate.

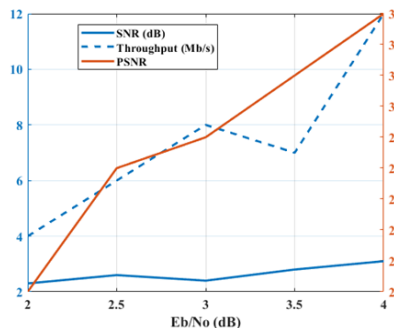


Fig. 8. SNR, PSNR and throughput of the proposed system

Fig. 8 analyzes the Signal-to-Noise Ratio (SNR), Peak Signal-to-Noise Ratio (PSNR) and throughput of the proposed method across varying SNR per bit values. The system achieves a maximum SNR of 3.1 dB at SNR per bit (E_b/N_0) of 4 dB, and a minimum of 2.3 dB at 2 dB. This improvement is due to the FTD, which minimizes packet loss and enhances data reliability, increasing SNR. In case of PSNR, a maximum PSNR of 33 is achieved at 4 dB SNR per bit, and a lower PSNR of 24 at 2 dB. This improved PSNR is largely recognized by modified RS codes in the proposed system which detects and corrects errors, reducing the error rate, resulting in higher PSNR values, hence a clearer and more accurate received signal.

On the other hand, at SNR per bit 2 dB, the system achieves a minimum throughput of 4 Mb/s, and at 4 dB, it reaches a maximum of 12 Mb/s. This increase in throughput is largely due to the APC-Rpt, which enhances the efficiency of decoding error-corrected data which minimizes retransmissions and optimizes data flow, directly contributing to higher throughput.

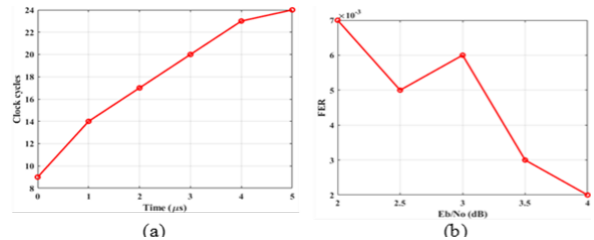


Fig. 9. (a) Clock cycle (b) FER of the proposed system

Fig. 9 (a) shows the clock cycle count of the proposed system corresponding to CPU execution time. At $5 \mu\text{s}$, the clock cycle count reaches a maximum of 24, while at $1 \mu\text{s}$, it decreases to 14 clock cycles. This reduction in clock cycles with shorter time periods is primarily due to the PCE and FTD, which optimize data processing that reduce the clock cycle and increases data encoding and decoding efficiency. The higher transistor switching speeds and more efficient data handling, contribute to an overall increase in processing speed, enabling the CPU to execute instructions with fewer clock cycles as time intervals decrease. Fig. 9(b) illustrates the Frame Error Rate (FER) performance of the proposed system across varying SNR per bit levels. At an SNR per bit of 4 dB, the FER reaches a minimum of 0.001, while at 2 dB, it achieves a maximum FER of 0.007. This reduction in FER at higher SNR levels, with a 2.5 to 3 dB variation is primarily due to the FTD, which effectively identify and correct errors in the received data, thus, decreasing the possible frame errors, even under challenging SNR conditions.

C. Comparison of Proposed Model with Previous Models

This section emphasizes the effectiveness of the proposed model by comparing it with the outcomes of existing techniques such as Polar [26] [27], Low-density parity check (LDPC), Tailbiting convolutional codes (TBCC), Turbo [26], Reed-Solomon codes (RS) [27], Unequal Error Protection scheme (UEP), Equal Error Protection (EEP) [28], Conventional Adaptive FEC, and Packet-Level FEC [29] to highlight its performance advantages over existing approaches.

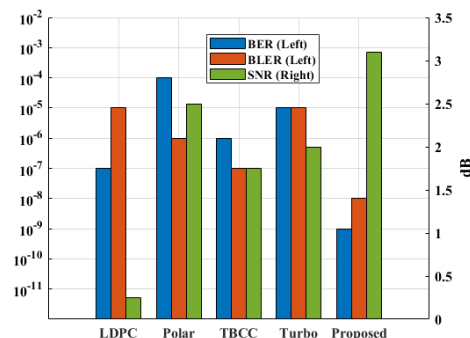


Fig. 10. Comparison of the BER, BLER and SNR

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Fig. 10 shows the BER, BLER and SNR of the proposed model compared to the existing models. For the current models LDPC, Polar, and Turbo, the BER values are 10^{-7} , 10^{-6} , and 10^{-5} , respectively, the BLER values are 10^{-5} , 10^{-4} , 10^{-6} , and 10^{-5} and the corresponding SNR are 0.25dB, 2.5dB, 1.75dB, and 2dB. However, the proposed model achieves a lower BER of 10^{-9} , low BLER of 10^{-7} , and a high SNR of 3.1dB in comparison to the existing models.

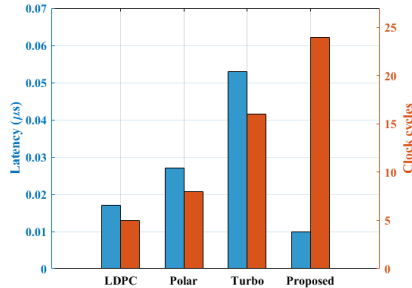


Fig. 11. Comparative analysis of the latency and clock cycle

Fig. 11 illustrates the comparison of the latency and clock cycle of the proposed model with existing models. The existing models such as LDPC, Polar, and Turbo achieves a latency of 0.017μs, 0.027μs, and 0.053μs and clock cycles of 5, 8, and 16 respectively. Compared with existing models the proposed model achieves a less latency of 0.01μs, and a maximum clock cycle of 24.

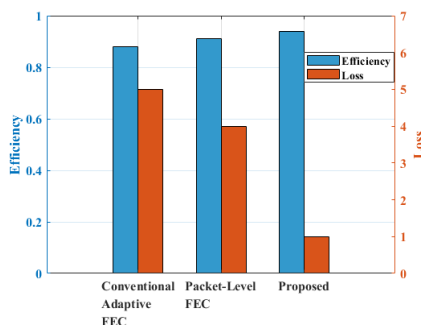


Fig. 2. Polarized Convolutional Encoder

The efficiency and loss of the suggested model is compared with existing models, as seen in Fig. 12. The efficiency of 0.88 and 0.91 and loss rates of 5% and 4% is achieved by the current models, Conventional Adaptive FEC and Packet-Level FEC. In comparison to current models, the proposed model attains a higher efficiency of 0.94 and a reduced 1% loss rate.

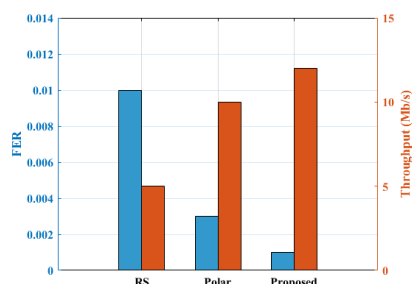


Fig. 12. Comparison analysis of the Efficiency and loss

Fig. 13 shows a comparison of the FER and throughput of the proposed model with the existing models. The FER for the current models such as RS and Polar are 1 and 0.003, respectively, and the corresponding throughput values of 5Mb/s and 10Mb/s. Compared with existing models, the proposed model achieves minimum FER of 0.001, and maximum throughput of 12Mb/s.

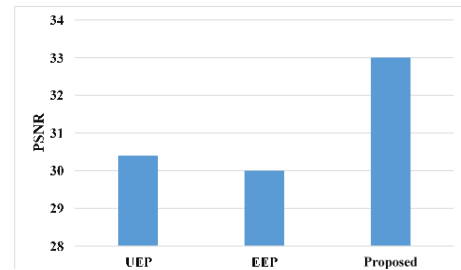


Fig. 14. Comparison of the PSNR of the proposed model

A comparison of the suggested model's PSNR with that of the current models is presented in Fig. 14. The current models' PSNR values are 30.4 and 30 for UEP and EEP. In contrast to current models, the suggested model attains a maximum PSNR value of 33.

V. CONCLUSION

In conclusion, the proposed CAPE-FID presented a promising solution to address the limitations of existing FEC techniques in wireless communication. By introducing a PCE and aFTD, the system effectively reduces latency, minimizes retransmission, and enhances communication efficiency. Through AFPCand Sequential Concatenated Turbo coding, the approach optimizes error detection and correction processes, thereby improving data transmission quality and network congestion handling. The utilization of Matlab modeling and FPGA implementation underscores the practicality and feasibility of the proposed mechanisms in real-world applications. Thus, the results of the simulation demonstrated that the proposed model has a low BER of 10^{-9} , BLER of 10^{-7} , FER of 0.001, Latency of 0.01μs, Loss of 1%, and high Clock cycles of 24, Efficiency of 0.94%, SNR of 3.1dB, PSNR of 33, and Throughput of 12Mb/s when compared to the previous models. Overall, this innovative approach offers significant advancements in wireless communication systems, adopting improved data rates, enhanced bandwidth utilization, and improved transmission efficiency in diverse network environments.

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